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Vertical Type Organic Transistor Using C₆₀ and Its Application for OLET

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We have fabricated static induction transistor of vertical type using C₆₀ with high carrier mobility as n-type organic semiconductor material to improve the characteristics of organic transistor. The effects of thin film thickness and the rate of deposition on the current-voltage and on-off ratio of transistor were investigated. And, we also studied the surface morphology of C₆₀ layer under various deposition rate with AFM. The vertical type organic transistor using C₆₀ exhibited low operation voltage compared to the case of F16CuPc. Additionally, the light emitting transistor using the vertical type transistor and P3HT as a light emitting polymer was investigated.

Keywords: C₆₀; light emitting transistor; on-off ratio; operation voltage; vertical type transistor

INTRODUCTION

Organic thin film transistors (OTFTs) have been studied for organic light emitting diode, e-paper and information tag because of their large area coverage, structural flexibility, low temperature processing,

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low cost and simple process such as screen or ink jet printing methods. However, conventional organic field effect transistors (OFETs) have low-speed, low-power and high-resistivity because of their long channel length between drain and source electrodes. Vertical type static induction transistor (SIT) is a promising device to improve the problems because of the high-speed and high-power operation [1–6].

In this work, we have fabricated vertical type organic SITs using C_{60} fullerene with high mobility as n-type organic semiconductor material [7]. The organic light emitting transistor consisting of ITO/PEDOT-PSS/P3HT/ C_{60} /Al gate/ C_{60} /Al was also fabricated. We have investigated the effects of thin film thickness and the rate of deposition on I-V and on-off ratio characteristics. Additionally, the device performance of organic light emitting transistor was described.

EXPERIMENTAL

C_{60} fullerene (Aldrich, USA) was used as a n-type semiconductor material. Light emitting polymer, poly-3-hexylthiophene (P3HT) and poly(3,4-ethylenedioxy thiophene)-poly(styrenesulfonic acid) (PEDOT-PSS) as an hole injection material were purchased from Aldrich and Bayer Co. Ltd., respectively. Chloroform was distilled from first grade solvent purchased from the market. Indium-tin-oxide (ITO) coated glass substrate (Samsung Corning, Korea) with sheet resistance less than $20\ \Omega$ was cleaned ultrasonically with a series of organic solvents.

The structures of vertical type organic transistor and light emitting transistor are shown in Figure 1(a) and (b). C_{60} layers were fabricated onto the patterned ITO glass substrate using vacuum evaporation technique (ULVAC VTR-300M/1ERH evaporator) at approximately 10^{-6} Torr. Substrate temperature was room temperature during the evaporation. At the first, C_{60} was deposited onto the patterned ITO glass. The evaporation rate was maintained at $0.6\ \text{\AA}/\text{sec}$ or $1.5\ \text{\AA}/\text{sec}$. The thickness of C_{60} layer was approximately $1500\ \text{\AA}$ and $2000\ \text{\AA}$, respectively. Secondly, Al gate electrode was fabricated with the patterned mask of $100\ \mu\text{m}$ grid type. The second C_{60} layer was deposited in the same method of first C_{60} layer. Finally, Al source electrode was deposited. P3HT was spin-coated from chloroform solution at a speed of 3000 rpm for 60 sec. PEDOT-PSS was also spin coated at a speed of 1000 rpm for 60 sec. The I-V (current-voltage) and luminance characteristics were measured by Keithly 237 and 2400 programmable source meter and Newport 1830-C photodiode. The luminance property of light emitting transistor was obtained using an Acton 300i spectrofluorometer. The surface morphology of C_{60} layer under various deposition rates was investigated with atomic force microscope (Park Scientific Instrument, AFM).

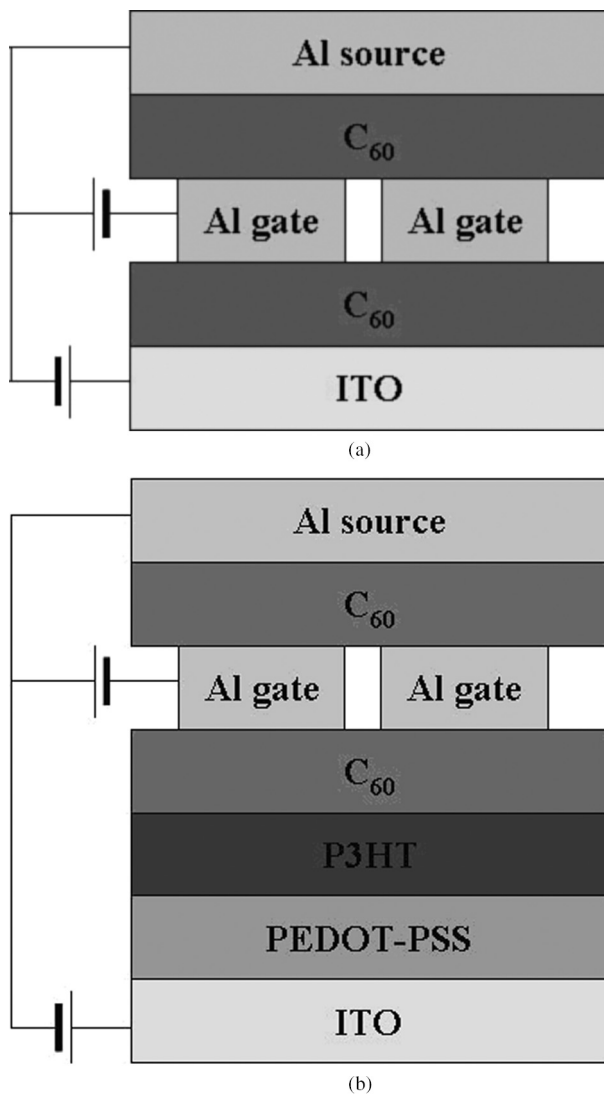


FIGURE 1 Schematic illustrations of (a) vertical type C_{60} transistor and (b) light emitting transistor.

RESULTS AND DISCUSSION

Figure 2 showed the current-voltage (I-V) characteristics of the vertical type transistor using C_{60} . In contrast to the saturation I-V characteristics of conventional MOS field effect transistors, no saturation

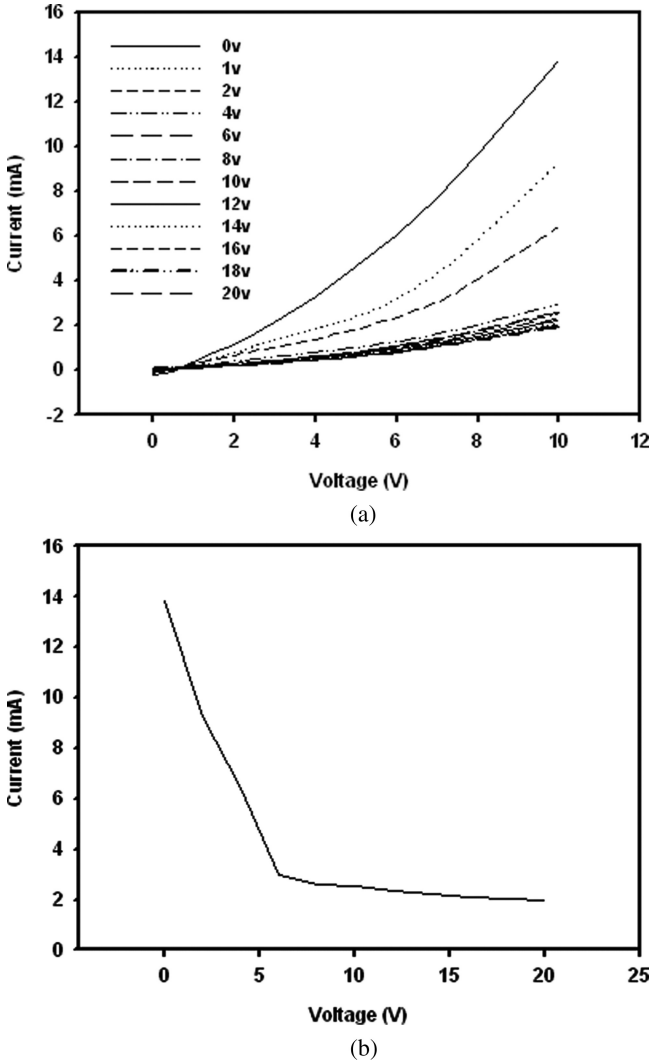


FIGURE 2 I-V characteristics of vertical type transistor consisting of Al/C₆₀/Al gate/C₆₀/ITO (a) Current-voltage characteristics; (b) Current-gate voltage characteristics.

occurs in the vertical type transistors. This is mainly due to the weak of negative feedback compared to the MOS field effect transistor. In other words, when the drain-source voltage (V_{DS}) in the vertical type transistor is increased, the drain-source current (I_{DS}) increases

TABLE 1 I-V and on-off Characteristics of Vertical Type Organic Transistors Under Various Thickness and Deposition Rates of C₆₀ Layers

Material	Thickness (Å)	Rate (Å/s)	Source-drain Voltage	Current (mA)	On/off ratio
C ₆₀	1500/1500	0.6	5 V	V _g = 0 V: 10.4105 V _g = 5 V: 5.2675	1.97
			2.5 V	V _g = 0 V: 3.6177 V _g = 5 V: 1.3963	2.59
C ₆₀	2000/2000	0.6	10 V	V _g = 0 V: 13.8363 V _g = 20 V: 1.9424	7.12
			5 V	V _g = 0 V: 4.6157 V _g = 20 V: 0.6317	7.31
C ₆₀	2000/2000	1.5	10 V	V _g = 0 V: 0.6656 V _g = 20 V: 0.1582	4.21
			5 V	V _g = 0 V: 0.2646 V _g = 20 V: 0.0379	6.98

exponentially. I_{DS} at a constant V_{DS} decreased with increasing a gate voltage (V_G), implies that the injected carrier from the source to drain is decreased with the increasing of potential barrier owing to the applied gate voltage. Thus, it can be argued that the prepared vertical type organic transistor shows the depletion mode as like conventional MOS field effect transistor.

In order to explore the effects of the thickness and topology of C₆₀ thin film on the performance of the vertical type transistor, the deposition rate of C₆₀ is firmly controlled by 0.6 Å/sec or 1.5 Å/sec. Table 1 showed the results. When the thickness of C₆₀ layer was 2000 Å at the deposition rate of 0.6 Å/sec, the maximum on-off ratio of 7.2 was obtained. It is mainly caused to the small roughness and grain size of C₆₀ surface.

Figure 3 showed the AFM images of C₆₀ surface deposited at 0.6 Å/sec and 1.5 Å/sec. The roughness and grains size of C₆₀ surface deposited at 0.6 Å/sec were 31 Å and 800 Å, respectively, implies that the C₆₀ morphology fabricated at low deposition rate was very uniform compared to the case of high deposition rate.

Figure 4 showed the luminance-voltage (L-V) characteristics and quantum efficiency-voltage of organic light emitting transistor (OLET) consisting of ITO/PEDOT-PSS/P3HT/C₆₀/Al gate/C₆₀/Al. I_{DS} at a constant V_{DS} decreased with increasing V_G . OLET using C₆₀ exhibited higher current than that of other materials used in the previous work [8]. In addition, the device showed low turn-on voltage, and no luminance was also observed at a gate voltage of 7 V.

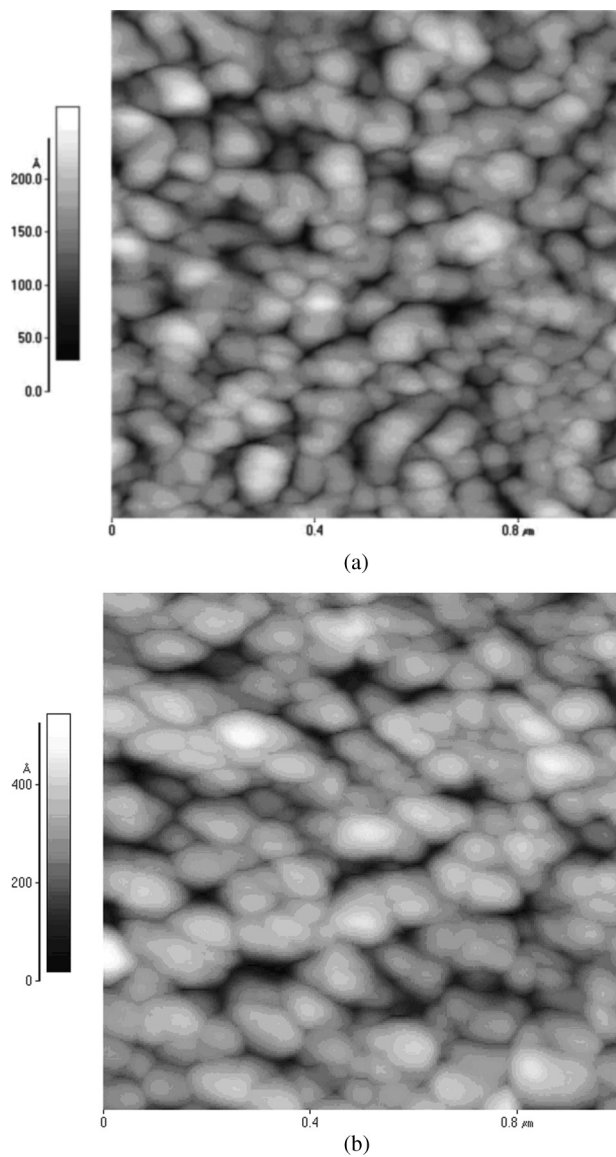
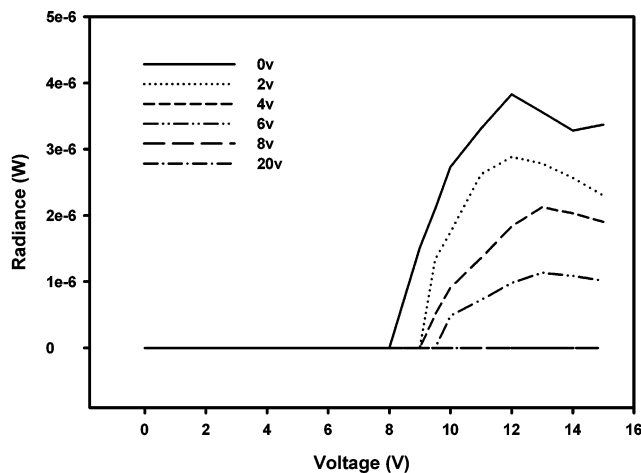
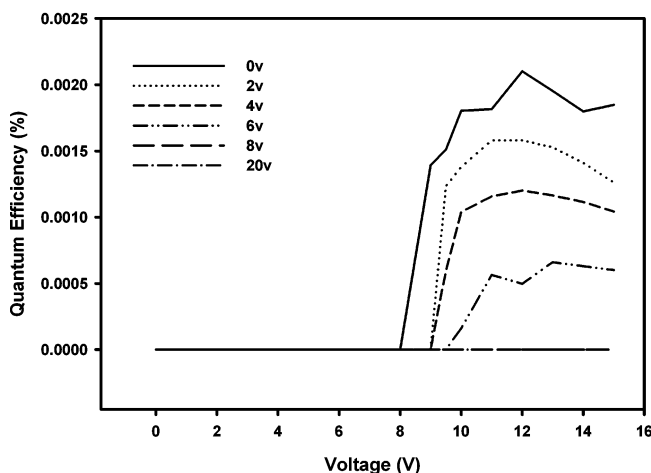


FIGURE 3 AFM images of C_{60} layers at the deposition rates of (a) 0.6 \AA/s and (b) 1.5 \AA/s .



(a)



(b)

FIGURE 4 Luminance-voltage characteristics (a) and Quantum efficiency consisting of ITO/PEDOT-PSS/P3HT/ C_{60} /Al gate/ C_{60} /Al (b).

CONCLUSIONS

Vertical type organic transistors using C_{60} were fabricated, and then the static induction transistor characteristics were examined. Relatively high current and on-off ratio (7.12) were observed in the vertical type transistor fabricated at the thickness of 2000 Å and the deposition rate of 0.6 Å/s. Additionally, light emitting transistor combined with

the vertical type transistor was successfully fabricated. It should be noted that the switching characteristic of light emitting transistor was observed at a gate voltage of 7 V.

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